REMARKS

This is in response to the Final Office Action of July 22, 2004. Claims 1-3, 5-13, and 15-24 were rejected. Claims 1, 10, 11, 20, 21, 22, and 24 were amended. Claims 2, 7-9, 12, and 18-19 were canceled.

The Examiner objected to a typographical error in claim 10. Applicant has made the requested change to claim 10 and corresponding changes to claim 20.

The Examiner rejected claims 6 and 16 on the basis that these claims are indefinite because they recite the trademark names MIPS32 and MIPS64. Applicant respectfully traverses the rejections of claims 6 and 16. Claims 6 and 16 include a limitation that the "kernel mode, said supervisor mode, said user mode, and said debug mode are based on a MIPS32™ or MIPS64™ architecture specification." Note that the claims are referring to particular architecture specifications. Applicant respectfully submits the claim scope is definite in this situation even though a trademark name is used to describe the type of architecture specification. MIPS Technologies, Inc. is in the business of designing processor architectures and cores that it licenses for use by others. The particular architectures are standardized for use by third parties in designing products. Each MIPS architecture is a standard that third parties design products around. The closest analogy to the MIPS architecture specifications would thus be an IEEE standard that companies design products around. Applicant therefore respectfully submits that a "MIPS32 architecture specification" or a "MIPS64 architecture specification" should be treated as standards that define a particular embodiment of a kernel mode, supervisor mode, and user mode. Applicant is submitting herewith as exhibits three articles that describe MIPS "industry standard" processor cores. The article "Zoran Corporation Takes Additional Licenses For Industry-Standard MIPS Cores," describes how MIPS Technologies is a provider of industry-standard processor cores. The article, "Industry Leadership To Market Leadership," describes how the MIPS architecture was developed over 20 years ago. The same article describes how MIPS licenses "its industry standard 32- and 64-bit ISAs." The article "MIPS32

Processor Architecture Adopted by Sony," describes how MIPS licenses "its industry-standard MIPS32® architecture."

In the Final Rejection the Examiner rejected the claims based upon new grounds in view of Alpert (U.S. Patent 5,621,886). Claims 1-3, 5, 7-9, 11-13, 15, 17-22, and 24 were rejected as being anticipated by Alpert. Claims 6 and 16 were rejected as being obvious over Alpert in light of "Embedded Processor Watch." Claims 10 and 20 were rejected as being obvious over Alpert in view of "MIPS R10000 Microprocessor User's Manual." Claim 23 was rejected as being obvious over Alpert.

Applicant respectfully submits that dependent claims 7, 10, 17, and 20 describe patentable subject matter and has consequently amended the independent claims to include aspects of these limitations. Applicant believes that the Examiner may have overlooked some aspects of claims 7, 10, 17, and 20 due to the language that was used and the length of the equations in claims 10 and 20. Therefore, Applicant has also amended the independent claims to make the relationships between elements easier to read.

Applicant has amended independent claims 1, 11, 21, 22, and 24 to include the limitation of claim 7 that the operating state includes an identity of a current process. Applicant has also incorporated some of the language of claims 2 and 10 to clarify that tracing is triggered based on a logical comparison of a current processor mode and a current ASID value to received control signal values.

While this amendment is fully supported by the original claims previously considered by the Examiner, additional support is found throughout Applicant's specification. As described in paragraph [1117], in a multi-tasking system each task or process has its own ASID value. The ASID value can be used in the debugging process to identify particular processes that need to be debugged. As described in paragraph [1119], in one embodiment tracing is triggered using a logical condition in which the current ASID value is compared to an ASID control signal and the processor mode is compared to a processor mode control signal.

One benefit of Applicant's claimed invention is that tracing is triggered for pre-selected logical combinations of processor modes and individual tasks. Thus, in Applicant's invention a

logical condition can be defined in which tracing is automatically triggered when the processor changes modes or when a particular task is running on the processor.

Alpert, the principal reference, does not teach or suggest triggering tracing based on the identity of a task being run on the processor. The other cited references also fail to teach this limitation. Consequently, Applicant respectfully submits that Applicant's claimed invention includes an element not taught or suggested by the prior art of record.

In the rejection of claim 7 the Examiner cited column 5, lines 55-57 and column 6, lines 1-3 of Alpert. (The Examiner provided no citations within Alpert in his rejection of claims 10, 17, and 20) Column 5, lines 55-57 describe "storing status information concerning the process currently executing on execution unit 142." However, while status information is stored, there is no teaching or suggestion in the cited sections of Alpert that tracing is triggered based on the ASID value of the current task.

Column 6, lines 1-3 of Alpert describe a processor with a user mode and a kernel mode. While Alpert discloses in column 8, lines 63-67 enabling debug events in the kernel mode and the user mode, Applicant can find no portions of Alpert that suggest triggering tracing based on ASID values.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is now in condition for allowance. The Examiner is invited to contact the undersigned if there are any residual issues that can be resolved through a telephone call.

The Commissioner is hereby authorized to charge any appropriate fees to Deposit Account No. 03-3117.

Dated: **November 22, 2004**

Respectfully submitted,
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EXHIBIT 1

ClariNews **Hot News** Special Edit

Zoran Corporation Takes Additional Licenses For Industry-Standard MIPS Cores

Story from MIPS Technologies via BizWire

Monday, 22-Sep-2003 6:41AM PDT

MOUNTAIN VIEW, Calif.--(BUSINESS WIRE)--Sept. 22, 2003--

MIPS32(TM) 4KE(TM) Family and M4K(TM) Core Provides Zoran

Additional Capabilities To Penetrate High-Growth Embedded Markets

Using MIPS-Based(TM) Technology

MIPS(R) Technologies, Inc. (Nasdaq: MIPS, MIPSB), a leading provider of industry-standard processor architectures and cores for digital consumer and business applications, announced today that Zoran Corporation has taken additional licenses for the high-performance MIPS32(TM) 4KE(TM) cores, and a new license for the 32-bit M4K(TM) core. These new agreements broaden Zoran's adoption of the industry-standard MIPS(R) architecture as the company continues to develop leading solutions for high-growth embedded markets.

"Our MIPS-based product portfolio is growing as we experience strong market demand for technology that enables OEMs to meet the challenging requirements of the digital consumer marketplace," said Ram Ofir, vice

president engineering at Zoran Corporation. "Since announcing the original licensing agreement with MIPS Technologies just one year ago, we have introduced two new MIPS-based products. We look forward to expanding our relationship with MIPS Technologies and to collaborating on the development of optimized solutions for the growing CE marketplace."

"Market leaders such as Zoran Corporation continue to standardize upon the MIPS architecture to leverage the broadly available software infrastructure that's only available for an industry standard," said Jack Browne, vice president of worldwide sales at MIPS Technologies. "With these new licenses, Zoran furthers its adoption of MIPS as it continues to gain market share in leading-edge DVD devices, digital cameras and high-definition televisions."

About MIPS Technologies

MIPS Technologies, Inc. is a leading provider of industry-standard processor architectures and cores for digital consumer and business applications. The company drives the broadest architectural alliance that is delivering 32- and 64-bit embedded RISC solutions. The company licenses its intellectual property to semiconductor companies, ASIC developers and system OEMs. MIPS Technologies and its licensees offer the widest range of robust, scalable processors in standard, custom, semi-custom and application-specific products. The company is based in Mountain View, Calif., and can be reached at 650-567-5000 or www.mips.com.

ClariNet Home

EXHIBIT 2

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MIPS32® Processor Architecture Adopted by Sony

TOKYO, Japan, May 17, 2004 - MIPS Technologies, Inc. (Nasdaq: MIPS), a leading provider of industry-standard processor architectures and cores for digital consumer and business applications, today announced it has licensed its industry-standard MIPS32® architecture to Sony Corporation.

"For decades, the MIPS architecture has been the technology-of-choice for the digital consumer marketplace." said Jack Browne, vice president of worldwide sales at MIPS Technologies. "Using our 32-bit architecture as the basis for their next-generation of processor cores, our licensees will be able to leverage the technology's high performance characteristics and unique features to develop products that meet the demanding requirements of consumer devices."

About the MIPS32 Architecture

The MIPS32 architecture sets a new performance standard for 32-bit embedded microprocessors. As a foundation of MIPS Technologies' roadmap, it provides upward compatibility to the MIPS64® architecture and features a robust instruction set of powerful instructions specifically designed for a wide spectrum of embedded applications. Today, MIPS Technologies' licensees are using the MIPS32 architecture and its core derivatives to develop a range of embedded applications ranging from ultra low power devices, such as smart cards and digital cameras, to high performance printers, copiers and digital televisions.

About MIPS Technologies

MIPS Technologies, Inc. is a leading provider of industry-standard processor architectures and

cores for digital consumer and business applications. The company drives the broadest architectural alliance that is delivering 32- and 64-bit embedded RISC solutions. The company licenses its intellectual property to semiconductor companies, ASIC developers and system OEMs. MIPS Technologies and its licensees offer the widest range of robust, scalable processors in standard, custom, semi-custom and application-specific products. The company is based in Mountain View, Calif., and can be reached at +1 (650) 567-5000 or www.mips.com.

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EXHIBIT 3

Corporate
About Us

- Our Business
- MIPS-Based™ Products
- Market Leadership
- Why MIPS
- Our Products
- Configurable Solutions

We are a leading provider of industry-standard processor architectures and cores for digital consumer and business applications.

Did You Know...
If you have a digital set-top box, chances are it's MIPS-Based™.
Your email very likely travels through a MIPS-Based Cisco router.
Your company's laser printers are probably powered by 64-bit MIPS-Based processors.

Industry Leadership to Market Leadership

The embedded industry is experiencing dynamic change driven by increasing demand for more information, better services and media-rich content with increased security in a wide range of products. To meet these trends, system OEMs and semiconductor companies are turning to industry-standard intellectual property (IP) that offers **proven, programmable high-performance** technology and enables **faster time to market**.

And, for an increasing number of industry leaders, the industry-standard microprocessor architecture they have come to rely on is the **MIPS® architecture**, which enables SOC design at a **fraction of the development cost** when compared to internally developed solutions.

At the heart of MIPS technology is the MIPS architecture, developed 20 years ago by Stanford University engineering professor John Hennessy, now president of Stanford. Hennessy took the lead in RISC processing and created an elegant, streamlined architecture with a scalability that has met the demands of generations of applications, thus preserving the wealth of development tools and software that support them.

Today, the MIPS architecture is an industry standard and **the performance** leader within the embedded industry. Backed by a vast ecosystem of companies dedicated to **best-in-class development support**, customers have confidence in bringing superior products to market on time, with **less risk** and **lower cost**.

Our Business Model

MIPS Technologies is a leading provider of industry-standard processor architectures and cores for digital consumer and business applications. We **design and license** the industry's highest performance **32- and 64-bit** architectures and cores, which also offer some of the **smallest silicon footprints** and **lowest power consumption** of any embedded microprocessors. Our customers include more than 100 of the world's leading OEM, fabless and ASIC semiconductor companies, and our technology is driving many high-growth embedded markets including digital set-top boxes, digital televisions, DVD recordable devices, broadband access devices, digital cameras, laser printers and network routers.

MIPS-Based™ Products

Our product offering is the broadest in the IP business, and includes optimized architectural extensions - such as those for programmability, multi-threading and security - and software solutions. And, by being the only company to openly license its industry-standard 32- and 64-bit ISAs, there are **hundreds of CPUs, ASSPs, ASICs, and hard and soft cores** now shipping to market - more than for any other embedded RISC architecture. These MIPS-Based products range from **ultralow-power CPU cores** occupying less than a half-millimeter of silicon to **quad-issue CPUs running at 1 GHz**. To date, our customers have shipped **over $1 billion worth of MIPS-Based silicon**.

Market Leadership

The MIPS® architecture drives the broadest range of 32- and 64-bit embedded solutions. We and our licensees target the largest markets for embedded applications - digital consumer devices and the networks that connect them - resulting in millions of MIPS-Based products around the world, including broadband devices from **Linksys**, digital cameras from **Canon**, DTVs and entertainment systems from **Sony**, DVD Recordable devices from **Pioneer**, digital set-top boxes from **Motorola**, network routers from **Cisco** and laser printers from **Hewlett Packard**.

In fact, MIPS is the **#1 architecture** in several high-volume, high-growth market segments, including:

- **Cable Modems** 94%
- **DSL Modems** 40%
- **VDSL Modems** 93%
- **IDTV** 40%
- **Cable STBs** 76%
- **DVD Recorder** 75%
- **Game Consoles** 76%
- **Office Automation** 48%
  - **Color Laser Printers** 62%
  - **Commercial Color Copiers** 73%

Source: Dataquest, IDC, Semico, In-Stat, Iconocast, MIPS Technologies
Values are percentage of WW box shipments

Why MIPS

Design engineers faced with the challenge of higher costs and shrinking market windows find a compelling solution in MIPS Technologies and MIPS-Based products. The MIPS advantage includes:

- Solutions that range from the highest performance to the lowest power consumption
- Open, licensable architecture for maximum design flexibility
- The broadest range of 32- and 64-bit CPUs, ASICs and cores
- Synthesizable and configurable cores
- Seamless 32-/64-bit compatibility to protect software investment
- Rapid, reliable, cost-effective development, supported by hundreds of tools and the most popular operating systems, including Linux, VxWorks and Windows CE

Our Products

Strong market demand for functions and applications that utilize digital-media and signal processing technologies are dramatically driving up the performance demands on SOCs. The result is a substantial growth in complexity of hardware and software solutions. Utilizing the inherent **performance** and **programmable** capabilities of the MIPS architecture, customers can **subsume peripheral logic functions**, such as digital signal processors, into their MIPS-Based core implementations.

Whether its ultralow power cores, optimized development tools and software, cacheless configurations, 64-bit cores with floating point or hard cores, MIPS Technologies offers the industry's broadest line of embedded microprocessors. Our products include:

- MIPS32® and MIPS64® instruction set architecture (ISA)
- Pro Series™ family of cores with CorExtend user-defined instruction capability
- Application Specific Extensions (ASE)
- MIPS32 4K™ and 4KE™ families of 32-bit cores
- MIPS32 M4K™ core
- MIPS32 4KS™ family of 32-bit cores
- MIPS32 24K™ family of 32-bit cores
- MIPS64 5K™ family of 64-bit cores
- System IP Solutions

Configurable Solutions

MIPS cores offer an extensive range of configurable options, giving design engineers enormous flexibility in their SOC designs. With our Pro Series™ cores, that flexibility is unlimited. Featuring the CorExtend™ capability, they are the only industry-standard cores that enable SOC designers to add instructions and functionality while maintaining compatibility with standard tool sets and software. For example, designers can boost performance by an order of magnitude, reduce power consumption, implement critical operations, and reduce overall product cost in ways that simply aren't possible with other industry-standard cores.

Important links
Highlights: A chronological history
Licensees: A list of our customers
Products: Description of our products

Financial information
Our fiscal year ends on June 30. MIPS Technologies' stock is traded on the Nasdaq stock market under the symbol "MIPS".

Membership/Affiliation
EEMBC
FSA
OCP IP

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